Remarks/Arguments

In the Non-final Office Action dated February 27, 2009, it is noted that claims 1-14 are pending and that claims 1-14 are rejected. Claims 1 and 13 are independent.

In the present amendment, the specification has been amended to clarify the use of the term "Channels" to a passive form, which one of ordinary skill in the art would be familiar with as the term is generally used with computer systems. Additional grammatical and phraseology changes were made to improve the language.

Claims 1-14 have been amended to clarify the claim language and phraseology. Claim 1 has also been amended by clarifying that communication is between an IC and an external RAM instead of communication with an external DRAM. Basis for this amendment is found, e.g. on page 1, line 37 to page 2, line 10 of the original filed specification, where various example memories are described to which the invention is applicable. Claim 1 is also amended to clarify that the "data exchange between the IC and the external RAM necessitates at least two memory bank commands." This feature is supported by the original specification. For example, from Fig. 1 and the corresponding description, one of ordinary skill in the art can derive that for writing data to the external RAM at least an activate command, a write command and a precharge command are necessary.

Independent Claim 13 is likewise amended similarly as claim 1.

No new matter has been added to the specification or claims.

Rejection of claims 1, 3, 4, 6, 7, 10, 13 and 14 under 35 USC §103(a) as unpatentable over Mes (US 7,028,142) in view of Dowling (US 2002/0040429)

The newly cited reference Mes appears to describe a system and a method for reducing access latency to a shared program memory 102 (Abstract). The program memory 102 is shared by more than one processor 104 (col. 3, lines 2-11). A round robin algorithm is applied, for example so each processor has equal opportunity to request a program instruction fetch (col. 4, lines 11-55).

Also disclosed are a fetch buffer 152 and a prefetch buffer 154 for storing a plurality of instructions being used by the associated processors 104 and arbitrators 108, 202, 204, 206, 208 for arbitrating between a plurality of instructions. Mes also describes that an "instruction" relating to the memory access is for example a "branch" or "jump." Mes provides these examples at column 1, lines 38-39. One ordinarily skilled in the art recognizes that an "instruction" in Mes is a logical action of memory access. It is important to distinguish between the logical action of a memory access, i.e. "instruction" and the commands for carrying out the logical access.

In contrast to Mes applicant's claim 1 includes: prioritizing the transmitted memory bank commands on the basis of a static priority allocation; and further prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels.

As further clarified in claim 1 "data exchange between the IC and the external RAM necessitates at least two memory bank commands."

Thus, claim 1 provides that a memory instruction requires at least two memory bank commands. In Mes the instructions between multiple processors may be arbitrated, however, there is no teaching in Mes of the commands for carrying out the instructions being prioritized as in claim 1, where "data exchange between the IC and the external RAM necessitates at least two memory bank commands."

For example, in the invention of claim 1, if data is to be written to the memory (for example an instruction in Mes), the instruction needs several steps (commands) to be performed. Thus, claim 1 was clarified to include data exchange between the IC and the external RAM necessitates at least two memory bank commands.

Each step of an instruction is initiated by a command. For example, an Activate command to activate the corresponding row in the memory, a Write command to initiate the data transfer by transmitting the write command together with the column address in the memory, and a precharge command has to be sent to deactivate the open row and reset the memory (page 2, line 25 to page 3,

line 2). The commands for carrying out the instruction are distinguished from the instruction.

Accordingly, applicant's claim 1 recites the "prioritizing memory bank commands" and "further prioritizing the commands" because it is the commands themselves, as defined in the claimed invention, which are to be prioritized.

In contrast, Mes does not disclose or suggest prioritizing the commands as claimed by applicant. Mes is describing arbitrating between instructions from different processors. Even if Mes describes arbitrators for arbitrating between a plurality of instructions from different processors accessing the same memory, that is different from prioritizing the commands as claimed by applicant. Thus, applicant respectfully submits that the reliance on Mes as teaching the above features should be withdrawn.

Dowling is relied upon in the rejection to apparently teach using a DRAM. However, Dowling fails to teach or even suggest the above discussed features lacking in Mes. Therefore, the combination of references fails to teach or even suggest each and every feature found in claim 1 and the rejection should be withdrawn.

Since claim 13 includes apparatus features substantially similar to those found in claim 1, it is also submitted that the combination of references does not teach, show, or suggest all the elements of Applicants' claim 13, as such, claims 1 and 13 full satisfy the requirements of 35 U.S.C. § 103 and are patentable there under.

Claims 3, 4, 6, 7, 10 depend from claim 1 and include all the features discussed above with respect to claim 1. Claim 14 depends from claim 13 and includes all the features discussed above with respect to claim 13 (claim 1). Thus, it is respectfully submitted that these dependent claims are likewise allowable for the above reasons and because they each include additional features.

With regard to claim 2, it is respectfully submitted that applicant could not find a detailed discussion or rejection of this claim.

With regard to the remaining dependent claims it is respectfully submitted that none of the further references teach the features lacking in the combination of Mes and Dowling as discussed above. Thus, applicants essentially repeat the above arguments for each dependent claim and respectfully request each rejection be withdrawn.

Conclusion

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed to have been incurred by virtue of this amendment. However, if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832.

Respectfully submitted,

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